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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)	
MAT-8657US	
Application Number	Filed
10/524,203	**February 10, 2005**
First Named Inventor	
Hiroaki OZEKI	
Art Unit	Examiner
2611	**Kabir A. Timory**

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.7.1 Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

☒ attorney or agent of record.
Registration number **34,515**

☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

Signature

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Typed or printed name

610-407-0700
Telephone number

May 7, 2009
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☒ *Total of 5 forms are submitted

The issue, here, is whether one of ordinary skill in the art would modify a prior art frequency divider - that includes a frequency multiplier -- with a prior art reference that discloses a heterodyning multiplier. The Examiner argues that it is proper to combine a frequency multiplier reference with a heterodyning multiplier reference. The Examiner does not explain why one of ordinary skill in the art would combine a frequency multiplier reference with a heterodyning multiplier reference. Applicants believe the Examiner has erred on this point and are thus filing this Request for Pre-Appeal Brief Conference.

Applicants' claims have been rejected by combining the Admitted Prior Art (AAPA) with Takahashi (U.S. 5,732,068). Specifically, frequency multiplier 109 (AAPA, Fig. 5) has been combined with frequency divider 51 (Takahashi, Fig. 6).

Applicants' claim 1 recites a frequency divider with an output connected to a **frequency multiplier** as shown in Fig. 1. Specifically, Applicants' frequency multiplier produces a product between an input frequency and a multiplier value. Takahashi, however, teaches a frequency divider input to a **heterodyning multiplier**. Takahashi's heterodyning multiplier mixes two sinusoids to produce an error signal of the input signals.

Takahashi's frequency divider 51 divides the frequency of an input signal by ½. This reduced frequency signal is then multiplied with the output of heterodyning multiplier 40. Multiplier 52 is performing a heterodyning operation between the output of multiplier 40 and the output of frequency divider 51 to produce a signal with the sum and difference of the input frequencies (the difference signal is the error signal). This feature is at least supported in Col. 11, lines 40 through Col. 12, line 10 of Takahashi ("*the ½ frequency divider 51 has the frequency of the output signal of the variable frequency divider 50. The output signal of the ½ frequency divider 51 is applied to a multiplier 52. In addition, the output signal of multiplier 40 which corresponds to the real part is applied to the multiplier 52. The multiplier 52 serves as a phase comparator operating on the output signals of the multiplier 40 and the ½ frequency divider 51*"). For example, if the two input frequencies of multiplier 52 are 3000Hz and 5000Hz, then the output signal would include the difference of the two signals (2000Hz) which is the error. In general, the connection of Takahashi's divider

51 and multiplier 52 in Fig. 6 is a common configuration found in phase lock loops (PLL) wherein a phase difference (error) is computed between two signals.

Applicants' frequency divider 4 in Fig. 1 is similar to Takahashi's frequency divider 51. Applicants' frequency multiplier 5 as shown in Fig. 1, however, is different than Takahashi's multiplier 52. Applicants' frequency multiplier 51 inputs one signal (not two signals) and multiplies its frequency by a multiplier value. Thus, by connecting frequency divider 4 and frequency multiplier 5 in cascade, the frequency of the reference signal may be reduced in frequency and then increased in frequency respectively. For example, if the reference signal has a frequency of 5,000 Hz and the frequency divider has a divisor value of 5, then the 5,000 Hz signal will be reduced to 1,000 Hz. Furthermore, if the multiplier value of frequency multiplier 5 is equal to 10, then the 1,000 Hz signal will be increased to 10,000 Hz. This feature is found on page 3, lines 15-27 of Applicants' specification ("*frequency divider 4 divides the frequency of reference signal ... frequency multiplier 5 multiplies the divided frequency of the reference signal*").

On page 6, lines 10-13, the Official Action states that it would be obvious to combine Takahashi and AAPA to produce an error signal ("*obvious...in order to produce an error signal*"). This error signal is described in Takahashi where the heterodyning multiplier 52 outputs a phase error signal between the output of multiplier 40 and the output of frequency divider 51 (error between two input signals). In contrast, connecting Takahashi's frequency divider with AAPA's frequency multiplier, would not result in an error signal. An error signal can only be computed by comparing two or more signals. Applicants frequency multiplier cannot produce an error signal because it only has a single input (two signals are not compared to produce an error).

KSR requires this rejection to indicate whether the combination was obvious to a person of ordinary skill in the art and to explain. The Official Action does exactly what KSR says should <u>not</u> be done, namely to argue that the references are combinable because components of each reference produce Applicants' claim. Applicants have argued that the references are not combinable because the two references disclose completely different multipliers. The two multipliers function differently and produce different outputs. There is simply no way for one of ordinary

skill to take one component receiving input from one type of multiplier, and to connect that component to another type of multiplier (unless, of course, impermissible hindsight is being used).

RAE/so

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